

SYSTEM, METHOD AND PROGRAM PRODUCT FOR POSITIONING I/O

PADS ON A CHIP

Abstract of the Invention

Under the present invention, a proposed placement of I/O pads into one or more groups on a chip analyzed. Specifically, using resources such as a control file, cross-reference table, an I/O limit table, and an optional information file, a group switching current for each proposed I/O pad group is automatically calculated and compared to predetermined maximum switching current(s). If an I/O pad group exhibits a switching current that exceeds its predetermined maximum, corrective action is taken. Such action can include, for example, relocation of an I/O pad from an overloaded I/O pad group to another I/O pad group, insertion of an additional power pad into the overloaded I/O pad group, etc.